WHAT IS CLAIMED IS:

1. In a data acquisition unit, a self-tuning filter, comprising:

a digital clocking signal;

an input coupled to said digital clocking signal, whereby the input reads a value incident on the input when the digital clocking signal changes to a predetermined state; and

a clock-tunable filter coupled to said digital clocking signal, whereby the frequency of the clock-tunable filter is adjusted in relation to a sampling frequency at which the digital clocking signal operates.

2. The self-tuning filter of claim 1, wherein the clock-tunable filter is a low-pass filter.

3. The self-tuning filter of claim 1, further comprising a frequency multiplier coupled to said digital clocking signal and said clock tunable filter, whereby the frequency of the clock tunable filter is a multiple of the sampling frequency.

4. The self-tuning filter of claim 3, wherein the frequency multiplier is a phase-lock loop.

5. The self-tuning filter of claim 1, wherein the input is an input of the data acquisition device.

6. The self-tuning filter of claim 1, wherein the sampling frequency at which the digital clocking signal operates is equal to the frequency at which the digital clocking signal changes to the predetermined state.

7. The self-tuning filter of claim 1, wherein the value incident on the input is a signal originating at a sensor.

8. The self-tuning filter of claim 7, wherein the sensor is a pressure sensor.

9. The self-tuning filter of claim 1, wherein the sampling frequency varies.

10. The self-tuning filter of claim 9, wherein the sampling frequency varies as a function of a degree of rotation of a shaft.

11. In a data acquisition unit, a self-tuning filter, comprising:

a digital clocking signal;

an input coupled to said digital clocking signal, whereby the input reads a value incident on the input when the digital clocking signal changes to a predetermined state and the digital clocking signal changes to the predetermined state at a varying rate;

a phase-lock loop coupled to said digital clocking signal; and

a clock-tunable filter coupled to said phase-lock loop, whereby the frequency of the clock tunable filter is a multiple of the sampling frequency at which the digital clocking signal changes to the predetermined state.

12. A method of controlling the frequency of a clock-tunable filter, comprising:

sensing a frequency at which a digital clocking signal changes state, whereby said digital clocking signal causes an input to read a value incident on the input when the digital clocking signal changes to a predetermined state;

adjusting a frequency of a clock-tunable filter in relationship to the frequency at which the digital clocking signal changes state.

13. The method of claim 12, further comprising:

multiplying the frequency of the digital clocking signal to acquire a desired filter frequency; and

wherein said adjusting includes adjusting the frequency of the clock-tunable filter to equal the desired filter frequency.

14. The method of claim 12, wherein the digital clocking signal changes state at a varying rate.